

Detector Support Group

We choose to do these things "not because they are easy, but because they are hard". Weekly Report, 2022-06-15

Summary

<u>Hall A – GEn-II</u>

<u>Mindy Leffel</u>

• Measured, cut, and bundled 400 of 400 RG59 SHV cables

<u>Hall B – LTCC</u>

Brian Eng and Marc McMullen

• Continued prototyping a method of initializing, and storing, startup values for MFCs and DAQ – want to update file on value changes above a specified threshold

<u>Hall B – RICH-II</u>

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, and Marc McMullen

- Investigating updating the FPGA code for the hardware interlock system
 - Frequency and phase control of the SHT35 clock and data is desirable for testing sensor boards – would require code modifications to the FPGA Command Engine

<u>Hall C – NPS</u>

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, and Marc McMullen

- Developing hardware interlock LabVIEW program
 - ★ Wrote subVI to break out large arrays for display in Phoebus screens
 - * Tested and debugged code for calculation of relative humidity
- Developed detector model to be used for Ansys simulation includes photomultiplier tubes, supports for crystals, heat exchangers, and detector enclosure



NPS detector model optimized for Ansys simulation

1 DSG Weekly Report, 2022-06-15



- Developing Ansys Fluent thermal simulations which includes heat removal effects of heat exchangers
 - ★ Ran simulation: air velocity and temperature for each fan set to 10 m/s and 10°C, respectively preliminary temperature in the electronic volume was 23.88°C
 - ★ Ran simulations with four fans, each with an air velocity of 3.33 m/s; included heat exchanger plates at 10°C, and ambient temperature at 20°C – preliminary results for the electronic volume temperature was 21°C
 - Noticed in air velocity contour plot that the air was not flowing out of the fan enclosure to the electronic volume – investigation in progress
- Terminated and tested three Samtec connectors for one high voltage supply cable
- Testing high voltage supply cables using Python 32 of 40 cables tested

<u>Hall D – JEF</u>

Mary Ann Antonioli, Aaron Brown, George Jacobs, and Mindy Leffel

- ESR foil pre-shaping 1403 of 1600 complete
- Wrapped six crystals with ESR foil and Tedlar

EIC

Pablo Campero, Brian Eng

• Attended JLAB/BNL Engineering Meeting – need to generate more realistic cable services

DSG R&D – EPICS Alarm System

<u>Peter Bonneau</u>

- Debugging Phoebus alarm system EPICS softIOC
 - * The softIOC, developed using EPICS base 3.14, stopped working after an automatic computer system update
 - ★ Recompiling the EPICS base resolved the issue